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Zan Yang; Byeong Min; Gwan Choi;

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000

Pages:160 - 169

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2 Improving the quality of controls and reducing costs for on-site adjustments with emulation:an example of emulation in baggage handling

Rengelink, W.; Saanen, Y.A.;

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3 Emulation of the Sparcle microprocessor with the MIT Virtual Wires emulation system

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4 A Transaction-Based Unified Architecture for Simulation and Emulation

Hassoun, S.; Kudlugi, M.; Pryor, D.; Selvidge, C.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:

13 , Issue: 2 , Feb. 2005

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5 A layered adaptive verification platform for simulation, test, and emulation

Zambaldi, M.; Ecker, W.; Henftling, R.; Bauer, M.;

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Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 6 , Dec. 2000

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[\[Abstract\]](#) [\[PDF Full-Text \(116 KB\)\]](#) **IEEE JNL****2 Using background modes for testing, debugging and emulation of microcontrollers***Melear, C.;*

WESCON/97. Conference Proceedings , 4-6 Nov. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(696 KB\)\]](#) **IEEE CNF****4 Emulation techniques for microcontrollers***Melear, C.;*

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Pages:539 - 544

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2 Configurable multilayer CNN-UM emulator on FPGA

Nagy, Z.; Szolgay, P.; Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 50 , Issue: 6 , June 2003
Pages:774 - 778

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3 Design of FPGA-based emulator for series multicell converters using co-simulation tools

Ruelland, R.; Gateau, G.; Meynard, T.A.; Hapiot, J.-C.; Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 2003
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4 A novel scheme of implementing high speed AWGN communication channel emulators in FPGAs

Yongquan Fan; Zilic, Z.; Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 2 , 23-26 May 2004
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5 A fast hardware/software co-verification method for system-on-a-chip

by using a C/C++ simulator and FPGA emulator with shared register communication

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10 iSAVE: a behavioral emulator for in-system algorithm verification

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Pages:345 - 348 vol.1

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12 A novel approach to real-time verification of transport system design using FPGA based emulator

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13 Configurable multi-layer CNN-UM emulator on FPGA

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Pages:1251 - 1254 vol.3

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15 A hardware accelerator for DSP system design: University of Tehran DSP Hardware Emulator (UTDHE)

Mahdiany, H.R.; Hormati, A.; Fakhraie, S.M.;

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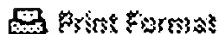
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